IN THE UNITED STATES PATEN	T AND TRADEMARK OFFICE
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Inventor Garo J. Derderian, et al. Assignee Micron Technology, Inc. Examiner T. Lee

Capacitor Fabrication Methods Including Forming a Conductive Layer Title:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

To:

Commissioner for Patents

PO Box 1450 Art Unit 2818

Alexandria, VA 22313-1450

From:

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449. Pursuant to 37 C.F.R. §1.98(a)(2)(1) no copies of any cited U.S. patents or U.S. published applications are included herewith. Copies of all other cited art references, if any, are attached. No admission is made regarding whether all the submitted references are prior art.

Citation of these references is respectfully requested.

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Respectfully submitted,

Date: 11 Mar 2005

Bv:

Reg. No. 44,854

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO. MI22-1330

SERIAL NO. 09/653,149

APPLICANT

Garo J. Derderian

FILING DATE

GROUP

	FILING 1 August 3			August 31, 2			GROUP 2818				
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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If Appropriate *Examiner Document Date Class Subclass Name Initial Number Agarwal (as amended 10/2003, 09/653,156 3/2004, and 12/2004) ΑB AC AD ΑE ΑF AG ΑH ΑI ΑJ ΑK FOREIGN PATENT DOCUMENTS Translation Document Date Class Subclass Country Number Yes No AL ΑM ΑN OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.) ΑO ΑP AQ **EXAMINER** DATE CONSIDERED

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